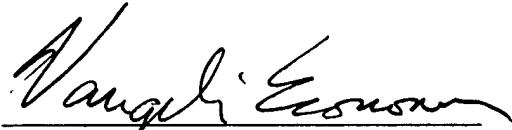


On the other hand, Claims 1, 11 and 13, as amended, specifically recite that "an upper end surface of each metal column (208) is substantially at the same level of height as an upper surface of the insulating layer 210". According to this feature, the metal column 208 is protected from an external force, which may be applied on the side surface. Accordingly, when mounting the semiconductor element 205 onto the wiring substrate 211, the metal column 208 is prevented from being disengaged from the uppermost interconnection layer 203a due to an external side force applied to the metal column 208.

Respectfully submitted,

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1. (Amended) A multilayer interconnection substrate comprising:

an uppermost interconnection layer having a plurality of terminal pads formed at positions corresponding to a plurality of external connection terminals provided on a semiconductor element which is to be mounted on said multilayer interconnection substrate;

a metal column formed on each of said terminal pads;

a resin film covering a side surface of said metal column; and

an insulating layer formed on said uppermost interconnection layer so that a gap is formed between the insulating layer and an outer peripheral surface of said resin film, wherein an upper end surface of each metal column is substantially at the same height as an upper surface of the insulating layer.

11. (Amended) A semiconductor device comprising:

a multilayer interconnection substrate which comprises an uppermost interconnection layer having a plurality of terminal pads formed at positions corresponding to a plurality of external connection terminals provided on a semiconductor element which is to be mounted on said multilayer interconnection substrate; a metal column formed on each of said terminal pads; a resin film covering a side surface of said metal column; and an insulating layer formed on said uppermost interconnection layer so that a gap is formed between the insulating layer and an outer peripheral surface of said resin film, wherein an upper end surface of each metal column is substantially at the same height as an upper surface of the insulating layer.

13. (Amended) a semiconductor device comprising:

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a multilayer interconnection substrate manufactured by forming a plurality of terminal pads in an uppermost interconnection layer; forming an insulating layer on said uppermost interconnection layer; forming openings in said insulating layer, the openings located at positions corresponding to said terminal pads; filling each of said openings with metal particles; forming a metal column in each of said openings by heating said metal particles at a temperature which melts said metal particles; and removing a part of said insulating layer near but not adjacent to a peripheral side of said metal column, while leaving a part of said insulating layer adjacent to said peripheral side of said metal column, so that a gap is formed around but not adjacent to said peripheral side of said metal column, wherein an upper end surface of each metal column is substantially at the same height as an upper surface of the insulating layer.